54.(New) The transistor of claim 50 wherein:

the gate comprises a floating gate; and

the transistor further comprises a polysilicon control gate separated from the floating gate by an intergate dielectric comprising oxide.

REMARKS

In response to the Office Action mailed January 18, 2000, the applicant requests reconsideration of the above-identified application in view of the following remarks. Claims 1-15 and 22-36 are pending in the application, and are rejected. Claims 6, 11, 14, 23, 25, 27-31, and 35 have been amended. New claims 37-54 have been added. No new matter has been added. None of the amendments to the claims have been made in response to the rejections based on prior art.

The Drawings

The drawings were objected to under 37 CFR 1.83(a). The applicant has added Figure 1A, showing a transistor according to one aspect of the invention, including a silicon carbide (SiC) gate and a semiconductor surface layer formed on an underlying insulating portion, to obviate the objection.

The applicant respectfully submits that no new matter has been added, based on *In re Heinle,* 145 USPQ 131 (CCPA 1965). The court in *In re Heinle* stated the following rule for amendments to the specification:

> "This is the familiar rule that the drawings and the specification may be amended to conform to each other and that the added matter will not be deemed technical "new matter" within the prohibition of the law. 35 USC 132." *In re Heinle,* 145 USPQ at 136.

The applicant respectfully submits that all of the elements shown in FIG. 1A were described on pages 6 and 7 of the specification, and that FIG. 1A does not contain new matter.

Information Disclosure Statement

The applicant filed a Supplemental Information Disclosure Statement on November 3, 1999. The Examiner returned a copy of the 1449 form with only one of the listed references

initialed. The citation of Fujii was not initialed by the Examiner to indicate that it has been considered. The applicant respectfully requests that Fujii be considered by the Examiner. Pursuant to the provisions of MPEP 609, the applicant further requests that a copy of the 1449 form filed on November 3, 1999, initialed by the Examiner to indicate that all listed citations have been considered, be returned with the next official communication.

Rejections Under 35 U.S.C. § 103

Claims 1, 4-11, 14, 15, 22-26, 29-32 and 35-36 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Japanese patent document 222367 to Oyama in view of the specification. The applicant respectfully traverses.

Claim 1 recites a transistor comprising a source region, a drain region, and a channel region between the source and drain regions in a semiconductor surface layer formed on an underlying insulating portion, and an electrically interconnected gate formed of a silicon carbide material.

Oyama is deficient in the following respects. Oyama discloses a transistor with a gate electrode of silicon carbide, but Oyama does not disclose a transistor in a semiconductor surface layer formed on an underlying insulating portion. The Examiner stated that pages 1-3 of the specification teach SOI structures. SOI technology is mentioned in the background of the specification, but there is no suggestion for the combination of the SOI technology and the transistor of Oyama put forward by the Examiner.

There must be a showing of a "teaching or motivation to combine prior art references" to support a rejection under section 103 and "the showing must be clear and particular." *In re Dembiczak,* 50 USPQ2d 1614, 1617 (Fed. Cir. 1999). Such a showing of a "teaching or motivation to combine" is necessary to avoid the use of hindsight when combining references under section 103. 50 USPQ2d at 1616-17.

SOI technology is mentioned in the background in the following paragraph:

> "One drawback of polysilicon gate FETs is that the V_T magnitude adjustment by ion-implantation is particularly difficult to carry out in semiconductor-on-insulator (SOI) and other thin film transistor technology. In SOI technology, the FET channel region is

> formed in a semiconductor layer that is formed upon an insulating region of the substrate. The semiconductor layer may be only 1000Å thick, making it difficult to obtain a sufficiently sharply defined dopant distribution through ion-implantation." Specification, page 2, lines 3-8.

Later, in the description of the invention, the applicant points out one advantage of an embodiment of the invention:

> "The SiC gate FET also provides lower V_T magnitudes without adjustment by ion-implantation. This is particularly useful for semiconductor-on-insulator (SOI) and other thin film transistor devices in which a sufficiently sharp doping profile is difficult to obtain by ion-implantation." Specification page 5, lines 21-25.

There is no suggestion, in either Oyama or the specification, for the combination put forward by the Examiner. The background indicates that polysilicon gate FETS have certain disadvantages when implemented in SOI technology, and says nothing about the claimed invention. The description indicates that a SiC gate FET is particularly useful for SOI technology. However, the description is not prior art, and cannot provide the motivation for a combination of prior art references. Therefore there is no teaching or motivation in either Oyama or the background of the application for the combination put forward by the Examiner.

The applicant respectfully submits that claim 1 is not disclosed or suggested by the combination of Oyama and the specification, and that claim 1 is in condition for allowance. For the reasons stated above, and the limitations in the claims, the applicant respectfully submits that claims 4-10, which are dependent on claim 1, are not disclosed or suggested by the cited references, and are also in condition for allowance. For the reasons stated above, and the limitations in the claims, the applicant respectfully submits that claims 15, 24-26, 29, and 30 are not disclosed or suggested by the cited references, and are also in condition for allowance.

Claim 11 recites an integrated circuit device comprising, among other elements, a p-channel transistor formed in a first portion of a substrate, the p-channel transistor including a silicon carbide gate, and an n-channel transistor formed in a second portion of the substrate, the n-channel transistor including a silicon carbide gate.

Oyama is deficient in the following respects. Oyama discloses a transistor with a gate

electrode of silicon carbide, but Oyama does not disclose a p-channel transistor and an n-channel transistor in the same substrate.

The Examiner stated that CMOS devices are well known. This may be true, but it does not supply a suggestion, as required by *Dembiczak*, for the use of the transistor of Oyama in a CMOS device.

The applicant respectfully submits that claim 11 is not disclosed or suggested by either Oyama or known CMOS devices, and that there is no suggestion for a combination thereof, and that claim 11 is in condition for allowance. For the reasons stated above, and the limitations in the claims, the applicant respectfully submits that claims 14, 22, and 23, which are dependent on claim 11, are not disclosed or suggested by the cited references, and are also in condition for allowance. For the reasons stated above, and the limitations in the claims, the applicant respectfully submits that claims 31, 32, 35, and 36 are not disclosed or suggested by the cited references, and are also in condition for allowance.

Claims 2, 3, 12, 13, 27, 28, 33, and 34 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Oyama in view of the specification, Halvis et al. (U.S. Patent No. 5,369,040, Halvis), and Chen et al. (U.S. Patent No. 5,714,766, Chen). The applicant respectfully traverses.

Claims 2, 3, 12, 13, 27, 28, 33, and 34 each recite one of polycrystalline silicon carbide and microcrystalline silicon carbide. The Examiner stated that Chen and Halvis disclose various forms of silicon carbide, and that the combination with Oyama and the specification is obvious. The applicant respectfully submits that the Examiner has not identified a clear and particular motivation for the combination as required by *Dembiczak*.

Furthermore, claims 2 and 3 are dependent on claim 1, claims 12 and 13 are dependent on claim 11, claims 27 and 28 are dependent on claim 15, and claims 33 and 34 are dependent on claim 31. For the reasons stated above, and the limitations in the claims, the applicant respectfully submits that claims 2, 3, 12, 13, 27, 28, 33, and 34 are not disclosed or suggested by the cited references, and are in condition for allowance.

C

CONCLUSION

The applicant respectfully submits that all of the pending claims are in condition for allowance, and such action is earnestly solicited. The Examiner is invited to telephone the below-signed attorney at 612-373-6973 to discuss any questions which may remain with respect to the present application. If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

LEONARD FORBES ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 373-6973

Date 18 APR 2000 By _____

Robert E. Mates
Reg. No. 35,271

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Assistant Commissioner of Patents, Washington, D.C. 20231 on **April 18, 2000**.

Susan Donovan
Name

Susan Donovan
Signature